Features

- **ARM7TDMI® ARM® Thumb® Processor Core**
- **One 16-bit Fixed-point OakDSPCore® Core**
- **Dual Ethernet 10/100 Mbps MAC Interface with Voice Priority**
- **Multi-layer AMBA™ Architecture**
- **256 x 32-bit Boot ROM**
- **88K Bytes of Integrated Fast RAM**
- **Flexible External Bus Interface with Programmable Chip Selects**
- **Codec Interface**
- **Multi-level Priority, Individually Maskable, Vectored Interrupt Controller**
- **Three 16-bit Timers/Counters**
- **Additional Watchdog Timer**
- **Two USARTs with FIFO and Modem Control Lines**
- **Industry Standard Serial Peripheral Interface (SPI)**
- **Up to 24 General-purpose I/O Pins**
- **On-chip SDRAM Controller for Embedded ARM7TDMI and OakDSPCore**
- **JTAG Debug Interface**
- **2.5V Power Supply for the Core and the PLL Pins, 3.3V for Other I/O Pins**
- **Software Development Suites Available for ARM7TDMI and OakDSPCore**
- **Supported by a Wide Range of Ready-to-use Application Software, Including Multitasking Operating System, Networking and Voice Processing Functions**
- **Available in a 208-lead PQFP Package**

Description

The AT75C220, Atmel's device in the family of smart Internet appliance processors (SIAP), is a high-performance processor specially designed for professional Internet appliance applications, such as the Ethernet IP phone. The AT75C220 is built around an ARM7TDMI microcontroller core running at 40 MIPS with an OakDSPCore co-processor running at 60 MIPS and a dual-port Ethernet 10/100 Mbps MAC interface.

In a typical standalone IP phone, the DSP handles the voice processing functions (voice compression, acoustic echo cancellation, etc.), while the dual-port Ethernet 10/100 Mbps MAC interface establishes the connection to the Ethernet physical layer (PHY), which links the network and the PC. In such an application, the power of the ARM7TDMI allows it to run a VoIP protocol stack as well as all the system control tasks.

Atmel provides the AT75C220 with three levels of software modules:

- A special port of the Linux kernel as the proposed operating system
- A comprehensive set of tunable DSP algorithms for voice processing, specially tailored to be run by the DSP subsystem
- A broad range of application level software modules such as H323 telephony or POP-3/SMTP e-mail services

Smart Internet Appliance Processor (SIAP™)

AT75C220

Preliminary

Rev. 1396BS–03/01

AT75C220 Pin Configuration

Table 1. AT75C220 Pin Configuration

Pin	Signal
1	GND
2	SCLKA
3	VDD3V3
4	FSA
5	STXA
6	SRXA
7	NTRST
8	MA_COL
9	MA_CRS
10	MA_TXER
11	MA_TXD<0>
12	MA_TXD<1>
13	MA_TXD<2>
14	MA_TXD<3>
15	MA_TXEN
16	VDD3V3
17	MA_TXCLK
18	GND
19	MA_RXD<0>
20	MA_RXD<1>
21	MA_RXD<2>
22	MA_RXD<3>
23	MA_RXER
24	MA_RXCLK
25	GND
26	VDD2V5
27	MA_RXDV
28	MA_MDC
29	MA_MDIO
30	MA_LINK
31	MB_COL
32	MB_CRS
33	GND
34	VDD2V5
35	VDD3V3
36	MB_TXER
37	MB_TXD<0>
38	MB_TXD<1>
39	MB_TXD<2>
40	GND
41	MB_TXD<3>
42	MB_TXEN

Pin	Signal
43	MB_TXCLK
44	MB_RXD<0>
45	MB_RXD<1>
46	MB_RXD<2>
47	MB_RXD<3>
48	MB_RXER
49	MB_RXCLK
50	MB_RXDV
51	MB_MDC
52	VDD3V3
53	GND
54	MB_MDIO
55	MB_LINK
56	A<0>
57	A<1>
58	A<2>
59	A<3>
60	A<4>
61	A<5>
62	A<6>
63	A<7>
64	A<8>
65	A<9>
66	A<10>
67	A<11>
68	A<12>
69	VDD3V3
70	GND
71	A<13>
72	A<14>
73	A<15>
74	A<16>
75	A<17>
76	A<18>
77	A<19>
78	A<20>
79	A<21>
80	D<0>
81	D<1>
82	D<2>
83	D<3>
84	GND

Pin	Signal
85	D<4>
86	VDD3V3
87	D<5>
88	D<6>
89	D<7>
90	D<8>
91	D<9>
92	D<10>
93	D<11>
94	D<12>
95	D<13>
96	D<14>
97	VDD2V5
98	GND
99	D<15>
100	VDD3V3
101	GND
102	NREQ
103	NGNT
104	VDD3V3
105	GND
106	DCK
107	CS0
108	CS1
109	RAS
110	CAS
111	NC
112	WE
113	DQM<0>
114	DQM<1>
115	DQM<2>
116	GND
117	DQM<3>
118	VDD2V5
119	GND
120	PLL_VDD
121	XREF240
122	PLL_GND
123	GND
124	XTALOUT
125	XTALIN
126	VDD2V5

Pin	Signal
127	NCE0
128	NCE1
129	NCE2
130	VDD3V3
131	NCE3
132	NWE0
133	NWE1
134	NWE2
135	VDD3V3
136	GND
137	NWE3
138	NWR
139	NSOE
140	GND
141	VDD2V5
142	NWAIT
143	MISO
144	MOSI
145	SPCK
146	NPCSS
147	VDD3V3
148	GND
149	RESET
150	FIQ
151	IRQ<0>
152	TST
153	GND
154	VDD2V5
155	NC
156	VDD3V3
157	GND
158	VDD3V3
159	TDO
160	TDI
161	TMS
162	TCK
163	PA<19>
164	VDD2V5
165	GND
166	PA<12>
167	GND
168	VDD3V3

Pin	Signal
169	PA<11>
170	PA<10>
171	PA<9>
172	PA<8>
173	PA<7>
174	PA<6>
175	VDD3V3
176	NC
177	PA<5>
178	PA<4>
179	PA<3>
180	PA<2>
181	PA<1>
182	PA<0>
183	GND
184	RXDA
185	TXDA
186	NRTSA
187	NCTSA
188	NDTRA
189	NDSRA
190	NDCDA
191	RXDB
192	TXDB
193	GND
194	PB<0>
195	PB<1>
196	PB<2>
197	PB<3>
198	PB<4>
199	PB<5>
200	PB<6>
201	PB<7>
202	PB<8>
203	PB<9>
204	VDD3V3
205	DBW32
206	GND
207	BO256
208	VDD3V3

Table 2. AT75C220 Pin Description List

Block	Pin Name	Function	Type
Common Bus	A[21:0]	Address Bus	Output
	D[15:0]	Data Bus	Input/Output
	NREQ	Bus Request	Input
	NGNT	Bus Grant	Output
Synchronous Dynamic Memory Controller	DCLK	SDRAM Clock	Output
	DQM[1:0]	SDRAM Byte Masks	Output
	CS0	SDRAM Chip Select 0	Output
	CS1	SDRAM Chip Select 1	Output
	RAS	Row Address Strobes	Output
	CAS	Column Address Strobes	Output
	WE	SDRAM Write Enable	Output
Static Memory Controller	NCE0, NCE3	Chip Selects	Output
	NWE[1:0]	Byte Select/Write Enable	Output
	NSOE	Output Enable	Output
	NWR	Memory Block Write Enable	Output
	NWAIT	Enable Wait States	Input
I/O Port A	PA[12:0]	General-purpose I/O lines. Multiplexed with peripheral I/Os.	Input/Output
	PA[19]	General-purpose I/O line. Multiplexed with peripheral I/Os.	Input/Output
I/O Port B	PB[9:0]	General-purpose I/O lines. Multiplexed with peripheral I/Os.	Input/Output
DSP Subsystem	OAKAIN[1:0]	OakDSPCore User Input	Input
	OAKAOUT[1:0]	OakDSPCore User Output	Output
Timer/Counter 0	TCLK0	Timer 0 External Clock	Input
	TIOA0	Timer 0 Signal A	Input/Output
	TIOB0	Timer 0 Signal B	Input/Output
Timer/Counter 1	TCLK1	Timer 1 External Clock	Input
	TIOA1	Timer 1 Signal A	Input/Output
	TIOB1	Timer 1 Signal B	Input/Output
Watchdog	NWDOVF	Watchdog Overflow	Output
Serial Peripheral Interface	MISO	Master In/Slave Out	Input/Output
	MOSI	Master Out/Slave In	Input/Output
	SPCK	Serial Clock	Input/Output
	NPCSS	Chip Select/Slave Select	Input/Output
	NPCS1	Optional SPI Chip Select 1	Output

Table 2. AT75C220 Pin Description List (Continued)

Block	Pin Name	Function	Type
USART A	RXDA	Receive Data	Input
	TXDA	Transmit Data	Output
	NRTSA	Ready to Send	Output
	NCTSA	Clear to Send	Input
	NDTRA	Data Terminal Ready	Output
	NDSRA/BOOTN	Data Set Ready	Input
	NDCDA	Data Carrier Detect	Input
USART B	RXDB	Receive Data	Input
	TXDB	Transmit Data	Output
JTAG Interface	NTRST	Test Reset	Input
	TCK	Test Clock	Input
	TMS	Test Mode Select	Input
	TDI	Test Data Input	Input
	TDO	Test Data Output	Output
Codec Interface	SCLKA	Serial Clock	Input/Output
	FSA	Frame Pulse	Input/Output
	STXA	Transmit Data to Codec	Input
	SRXA	Receive Data to Codec	Output
MAC A Interface	MA_COL	MAC A Collision Detect	Input
	MA_CRS	MAC A Carrier Sense	Input
	MA_TXER	MAC A Transmit Error	Output
	MA_TXD[3:0]	MAC A Transmit Data Bus	Output
	MA_TXEN	MAC A Transmit Enable	Output
	MA_TXCLK	MAC A Transmit Clock	Input
	MA_RXD[3:0]	MAC A Receive Data Bus	Input
	MA_RXER	MAC A Receive Error	Input
	MA_RXCLK	MAC A Receive Clock	Input
	MA_RXDV	MAC A Receive Data Valid	Output
	MA_MDC	MAC A Management Data Clock	Output
	MA_MDIO	MAC A Management Data Bus	Input/Output
	MA_LINK	MAC A Link Interrupt	Input

Table 2. AT75C220 Pin Description List (Continued)

Block	Pin Name	Function	Type
MAC B Interface	MB_COL	MAC B Collision Detect	Input
	MB_CRS	MAC B Carrier Sense	Input
	MB_TXER	MAC B Transmit Error	Output
	MB_TXD[3:0]	MAC B Transmit Data Bus	Output
	MB_TXEN	MAC B Transmit Enable	Output
	MB_TXCLK	MAC B Transmit Clock	Input
	MB_RXD[3:0]	MAC B Receive Data Bus	Input
	MB_RXER	MAC B Receive Error	Input
	MB_RXCLK	MAC B Receive Clock	Input
	MB_RXDV	MAC B Receive Data Valid	Output
	MB_MDC	MAC B Management Data Clock	Output
	MB_MDIO	MAC B Management Data Bus	Input/Output
	MB_LINK	MAC B Link Interrupt	Input
Miscellaneous	RESET	Power on Reset	Input
	FIQ/LOWP	Fast Interrupt/Low Power	Input
	IRQ0	External Interrupt Requests	Input
	XREF240	External 240 MHz PLL Reference	Input
	XTALIN	External Crystal Input	Input
	XTALOUT	External Crystal Ouptut	Output
	TST	Test Mode	Input
	B0256	Package Size Option (1 = 256 pins)	Input
	DBW32	External Data Bus Width for CS0 (1 = 32 bits)	Input

Block Diagram

Figure 1. AT75C220 Block Diagram

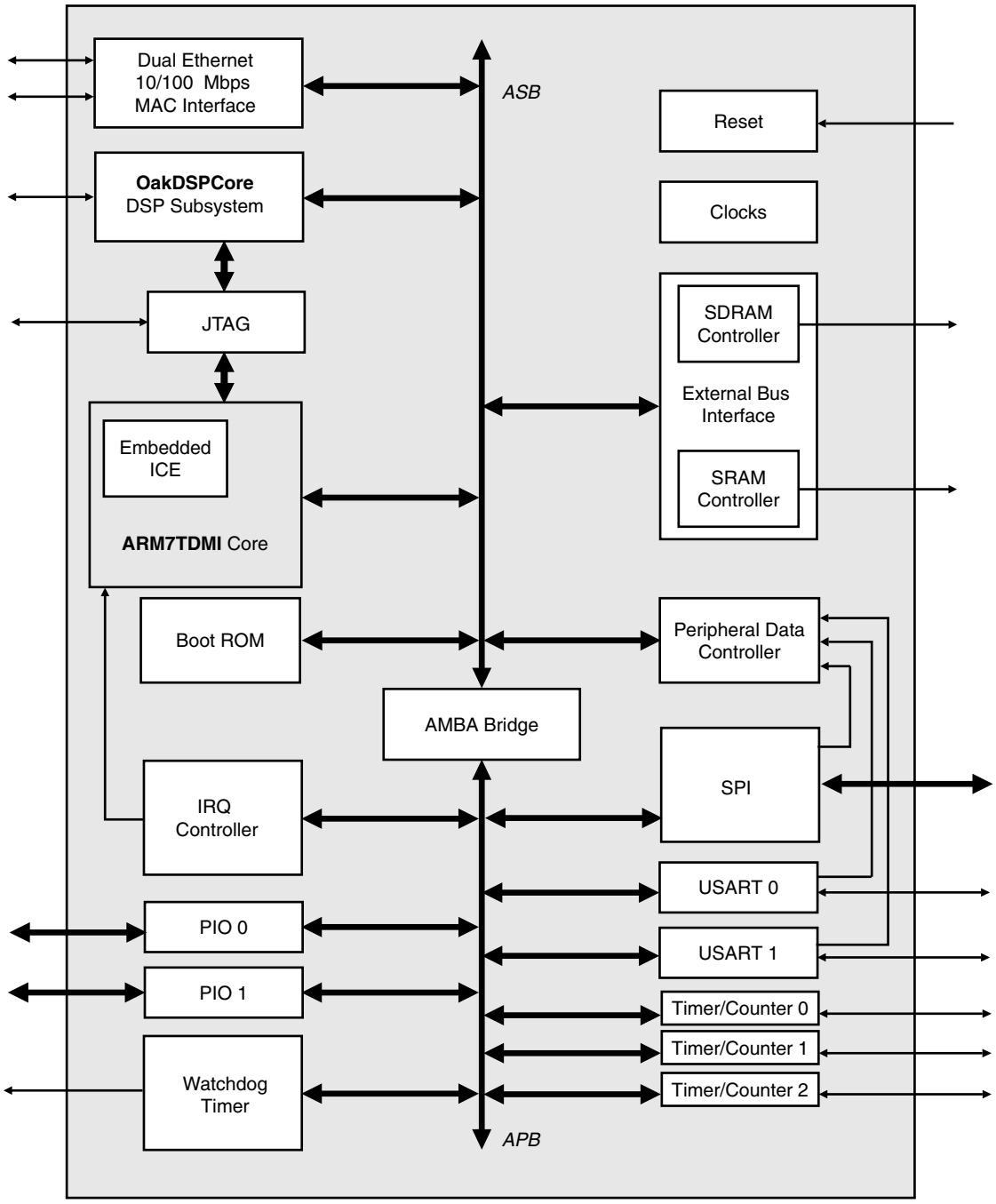
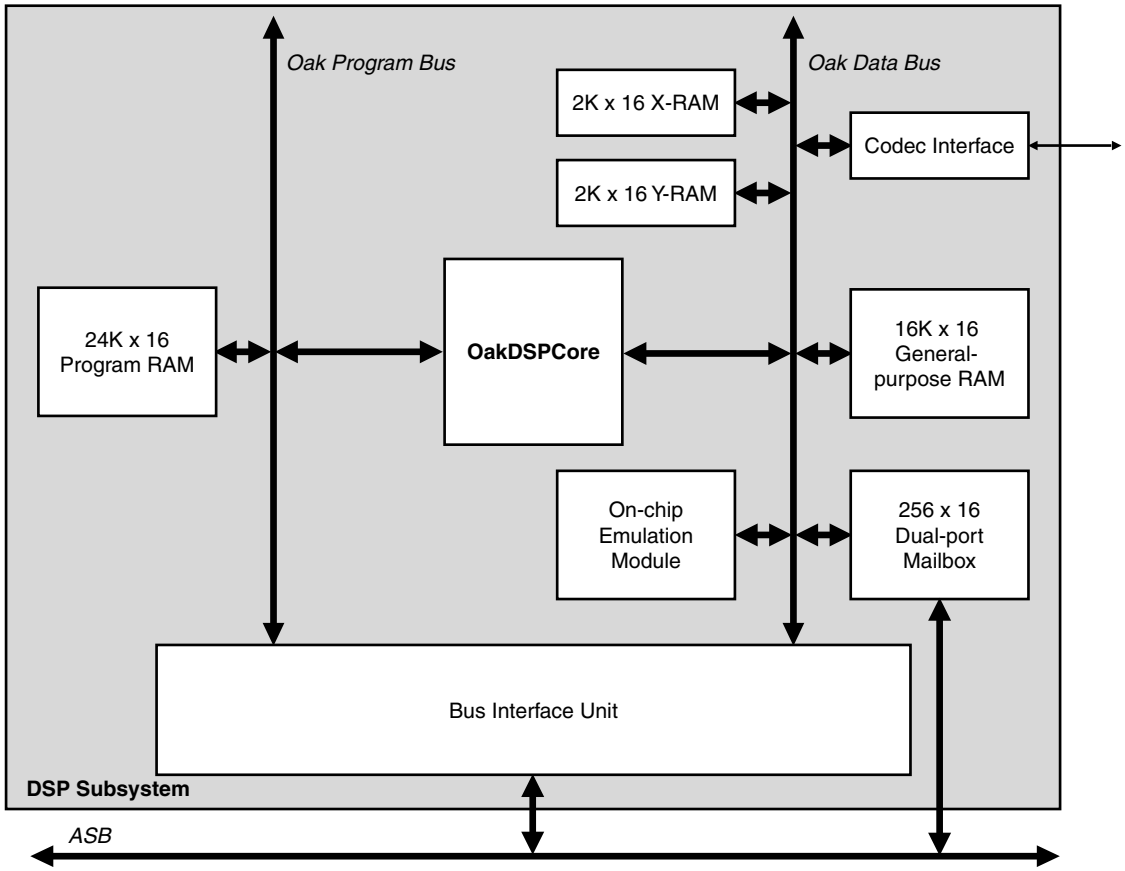
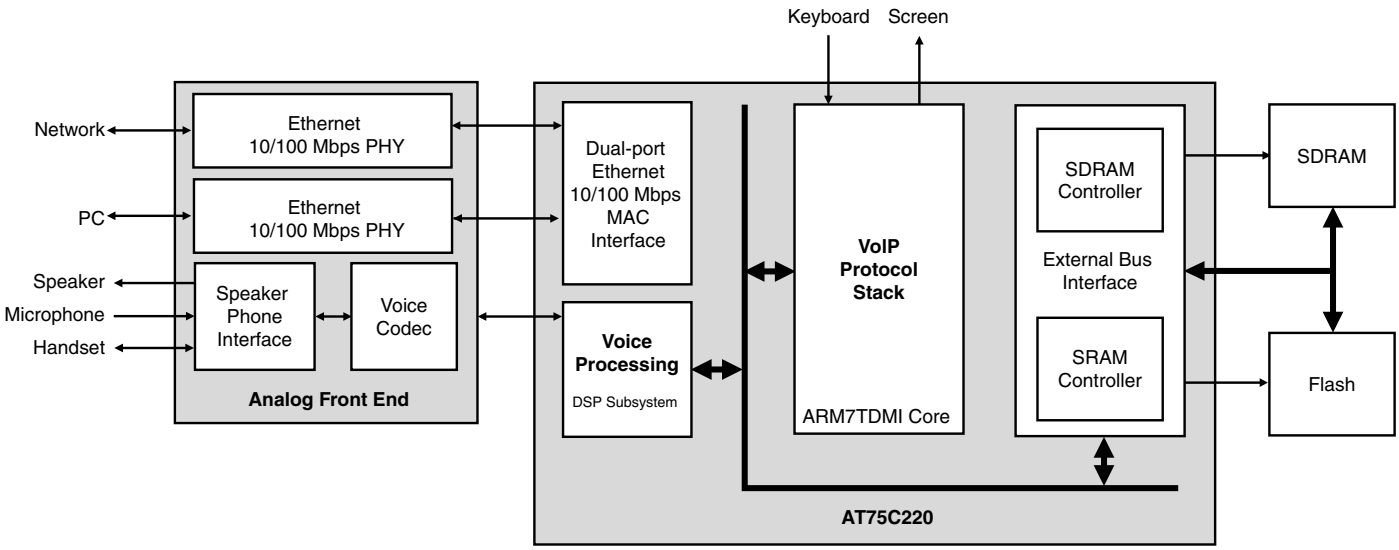


Figure 2. DSP Subsystem Block Diagrams



Application Example

Figure 3. Standalone Ethernet Telephone



Functional Description

ARM7TDMI Core

The ARM7TDMI is a three-stage pipeline, 32-bit RISC processor. The processor architecture is Von Neumann load/store architecture, characterized by a single data and address bus for instructions and data. The CPU has two instruction sets: the ARM and the Thumb instruction set. The ARM instruction set has 32-bit wide instructions and provides maximum performance. Thumb instructions are 16-bit wide and give maximum code density.

Instructions operate on 8-bit, 16-bit and 32-bit data types.

The CPU has seven operating modes. Each operating mode has dedicated banked registers for fast exception handling. The processor has a total of 37 32-bit registers, including six status registers.

DSP Subsystem

The AT75C220 DSP subsystem is composed of:

- An OakDSPCore running at 60 MIPS
- 2K x 16 of X-RAM
- 2K x 16 of Y-RAM
- 16K x 16 of general purpose data RAM
- 24K x 16 of loadable program RAM
- One 256 x 16 dual-port mailbox
- One codec interface

The DSP subsystem is fully autonomous. The local X- and Y-RAM allows it to reach its maximum processing rate, and a local large data RAM enables complex DSP algorithms to be implemented. The large size of the loadable program RAM permits the use of functions as complex as a low bit-rate vocoder.

During boot time, the ARM7TDMI core has the ability to maintain the OakDSPCore in reset state and to upload DSP code. When the OakDSPCore reverts to an active state, this code is executed.

When the OakDSPCore is running the dual-port mailbox is used as the communication channel between the ARM7TDMI and the OakDSPCore.

A programmable codec interface is directly connected to the OakDSPCore. It allows the connection of most industrial voice, multimedia or data codecs.

Ethernet MAC

The AT75C220 contains an Ethernet subsystem specially designed to cope with the VoIP application requirements. It is mainly composed of three independent parts: two identical independent Ethernet MACs and a packet buffer of 32K bytes, connected together with a local bus. The major benefit provided by two separate Ethernet MACs is the possibility to deploy VoIP Ethernet telephony without re-wiring buildings.

The Ethernet MACs exhibit the following features:

- Support for 10 and 100 Mbps operation
- Support for full- and half-duplex
- Standard MII interface
- Broadcast, multicast and four unicast address filters
- Automatic CRC generation
- Automatic zero padding

- Pause and jamming support
- Transmit and receive FIFOs
- Integrated DMA

The local packet buffer is filled/emptied by the MACs' DMA. This memory is used to store the received/transmitted packets temporarily. Its size allows it to hold enough packets to cope with most situations. Should an overflow occur, a part of the external system memory can be used as an overflow buffer to avoid data loss.

The main benefit of having a local bus is that the majority of packets can be received from one MAC and transmitted through the other without software intervention.

Boot ROM

The ARM7TDMI has the ability to boot either from an external memory or from the on-chip 256 x 32-bit boot ROM.

Boot Code Operation

The internal boot sequence allows programming of the ARM7TDMI program RAM through a serial port. When the download is complete, a branch is executed to the downloaded code.

EBI: External Bus Interface

The EBI generates the signals which control access to external memory or memory-mapped peripherals. The EBI is fully programmable and can address up to 64M bytes. The interface to external devices is composed of common address and data buses and separate control lines to allow the connection of static or dynamic devices.

The main features are:

- External memory mapping
- Up to four chip select lines
- 32- or 16-bit data bus
- Byte write or byte select lines
- Remap of boot memory
- Support for both static and dynamic memories
- Two different read protocols for static memories
- Support for early read/early write for dynamic memories
- Programmable wait state generation
- Programmable data float time

AIC: Advanced Interrupt Controller

The AT75C220 has an 8-level priority interrupt controller. The interrupt controller outputs are connected to the fast interrupt request (NFIQ) and the normal interrupt request (NIRQ) of the ARM7TDMI core. The processor's NFIQ can only be asserted by the external fast interrupt request input (FIQ). The NIRQ line can be asserted by the interrupts generated by the on-chip peripherals or by the external interrupt request line IRQ0.

An 8-level priority encoder allows the application to define the priority between the different interrupt sources. Interrupt sources are programmed to be level sensitive or edge sensitive. External sources can be programmed to be positive- or negative-edge triggered, or low- or high-level sensitive.

PIO: Parallel I/O Controller

The AT75C220 has 24 programmable I/O lines. They can all be programmed as inputs or outputs. To optimize the use of available package pins, most of them are multiplexed with external signals of on-chip peripherals.

The PIO lines are controlled by two separate and identical PIO controllers called PIOA and PIOB.

The PIO controllers enable the generation of an interrupt on input change on each PIO line.

Some I/O lines have enough drive capability to power a LED.

USART: Universal Synchronous/ Asynchronous Receiver/ Transmitter

The AT75C220 provides two identical full-duplex, universal synchronous/asynchronous receiver/transmitters that interface to the APB and are connected to the Peripheral Data Controller.

The main features are:

- Programmable baud rate generator
- Parity, framing and overrun error detection
- Line break generation and detection
- Automatic echo, local loopback and remote loopback
- Multi-drop mode: address detection and generation
- Interrupt generation
- Dedicated peripheral data controller channels
- 6-, 7- and 8-bit character length

Additionally to the Tx and Rx signals, the USART A provides several modem control lines.

SPI: Serial Peripheral Interface

The AT75C220 includes an SPI which provides communication with external devices in master or slave mode.

The SPI has one external chip select which can be connected to up to 2 devices. The data length is programmable from 8- to 16-bit.

Timer/Counter

The AT75C220 features three identical 16-bit timer/counters. They can be independently programmed to perform a wide range of functions, including frequency measurement, event counting, interval measurement, pulse generation, delay timing and pulse-width modulation.

The triple timer/counter block has three external clock inputs, five internal clock inputs and two multi-purpose signals which can be configured by the user. Each timer drives an internal interrupt signal which can be programmed to generate processor interrupts via the Advanced Interrupt Controller.

Watchdog Timer

The AT75C220 has an internal Watchdog Timer which can be used to prevent system lock-up if the software becomes trapped in a deadlock.

Special Functions

The AT75C220 provides registers which implement the following special functions:

- Chip identification
- Reset status
- Power management

Application Software

The AT75C220 is supported by a comprehensive range of software modules. As a result of the widespread use of the ARM7TDMI and the OakDSPCore, a wide range is available directly from Atmel, from Atmel's qualified software partner or from other third parties.

The application software modules are in three categories: OS, DSP and application levels.

OS Level

The AT75C220 is supplied with a customized port of the Linux kernel. It features device drivers for all the on-chip peripherals, including the DSP subsystems, and supports virtual file system usage. It also supports the native TCP/IP facilities which have made Linux a success in Internet applications. This kernel is available in source code under the terms of the Gnu Public License.

Many other operating systems exist for the ARM7TDMI core.

DSP Level

A wide range of digital signal processing functions is available for the OakDSPCore. Amongst others, Atmel supplies modules for G723.1 and G729A voice codecs, silence compression and echo cancellation.

Many third parties also provide ready-to-use libraries for the OakDSPCore.

Application Level

A rich software toolkit is available with support for popular communication protocols (H323, POP-3/SMTP, etc.), connection processes, multimedia applications, full-feature telephony and audio software suites.

Development Tools

Both the ARM7TDMI and the OakDSPCore are industry-standard cores. They are supported by a comprehensive range of state-of-the-art development tools, including assemblers, C-compilers, source level debuggers and hardware emulators.

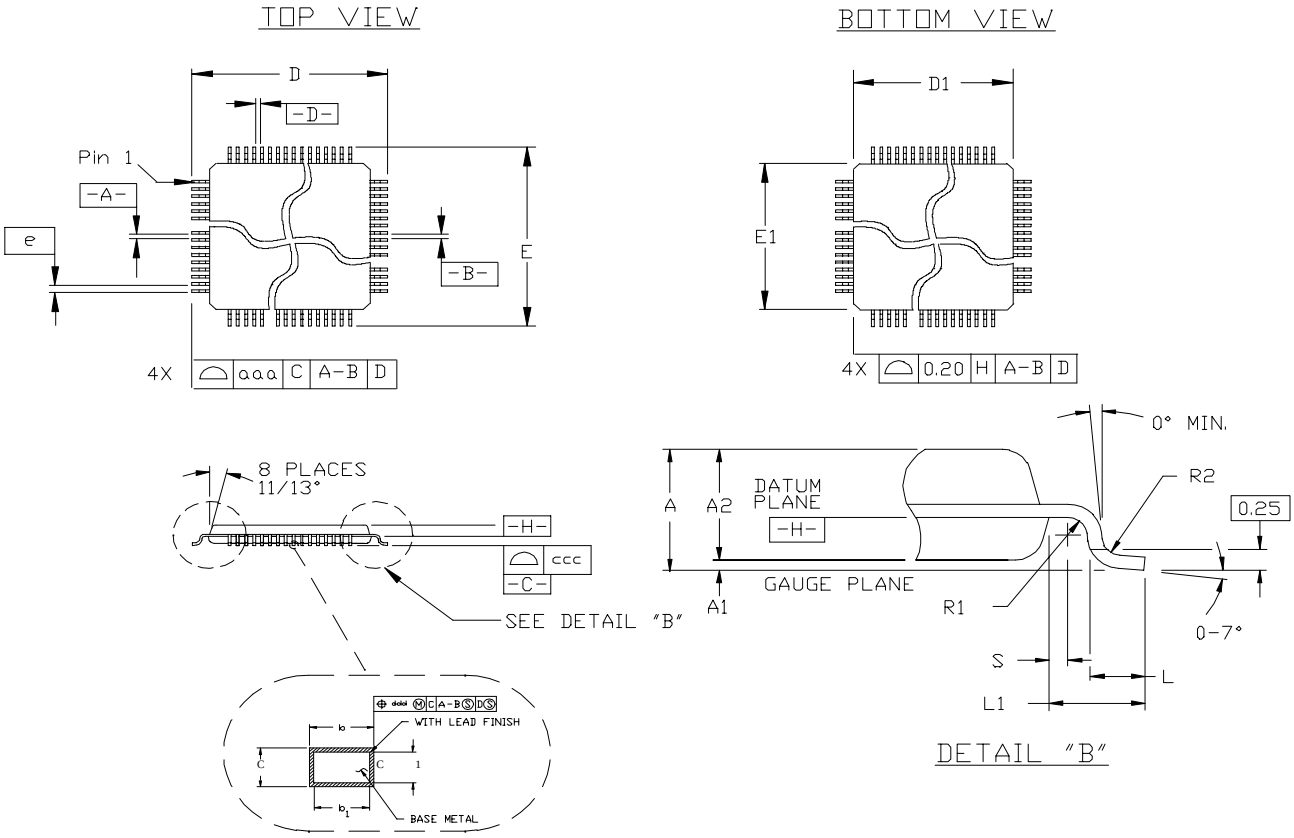
Packaging

The AT75C220 is supplied in a 208-lead PQFP package. This provides the best compromise between external connectivity and cost.

An alternative 256-ball PBGA package is also available. In addition to a larger I/O capability, it provides the application developer with the possibility of using advanced development tools for the DSP subsystem software.

Although this 256-ball PBGA package is more dedicated to development, it can also be used in production for systems which require a high level of connectivity: it offers up to 48 general-purpose I/Os and a full-width system bus (24 address bits and 32 data bits).

Figure 4. PQFP Package Drawing



For package data, see Table 3, Table 4 and Table 5 below.

Package Data

Table 3. Dimensions (mm)

Symbol	Min	Nom	Max
c	0.11		0.23
c1	0.11	0.15	0.19
L	0.65	0.88	1.03
L1		1.60 REF	
R2	0.13		0.3
R1	0.13		
S	0.4		
Tolerances of Form and Position			
aaa		0.25	
ccc			0.10

Table 4. Dimensions specific to 208-lead Package (mm)

A	A1	A2			b		b1			D	D1	E	E1	e	ddd
Max	Min	Min	Nom	Max	Min	Max	Min	Nom	Max	BSC	BSC	BSC	BSC	BSC	BSC
4.10	0.25	3.20	3.40	3.60	0.17	0.27	0.17	0.20	0.23	31.20	28.00	31.20	28.00	0.50	0.10

Table 5. 208-lead PQFP Package Electrical Characteristics

Body Size	R (mΩ)		C_s (pF)		C_m (pF)		L_s (nH)		L_m (nH)	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
28 x 28	53	71	1.4	1.7	0.56	0.73	6.7	8.4	3.9	5.1

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